

A

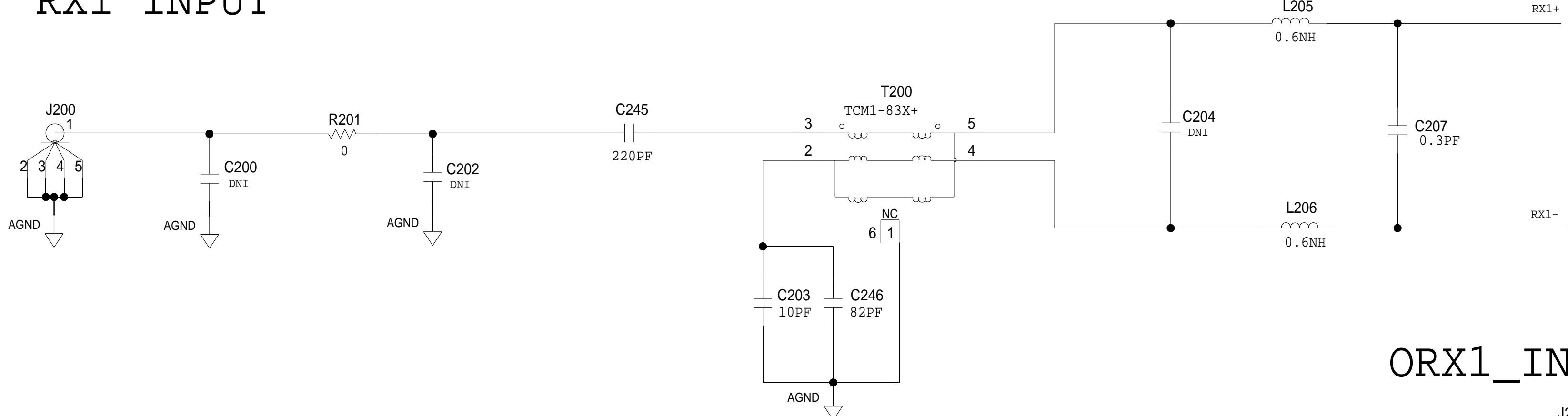


TEMPLATE ENGINEER	DATE	<div>SCHEMATIC</div> <div><div></div>ANALOG DEVICES</div> <div>HW TYPE : Customer Evaluation Z Product(s): AD9375</div> <div>PACKAGE : 196-lead 12X12_MM CBGA-family : Pitch-pitch StyleVendor Style</div>						
HARDWARE SERVICES								
HARDWARE SYSTEMS								
TEST ENGINEER								
COMPONENT ENGINEER								
TEST PROCESS								
HARDWARE RELEASE								
DESIGNER J BOWNE	17JAN17	MASTER PROJECT TEMPLATE TBD	TESTER TEMPLATE no_template	DRAWING NO. 02_047000			REV. B	
PTD ENGINEER T KARPUS	17JAN17	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES X.XX +0.010 +1/32 +2 X.XXX +0.005			SIZE D	SCALE 1:1	CODE ID NO. CodeID	SHEET 1 OF 8
CHECKER								

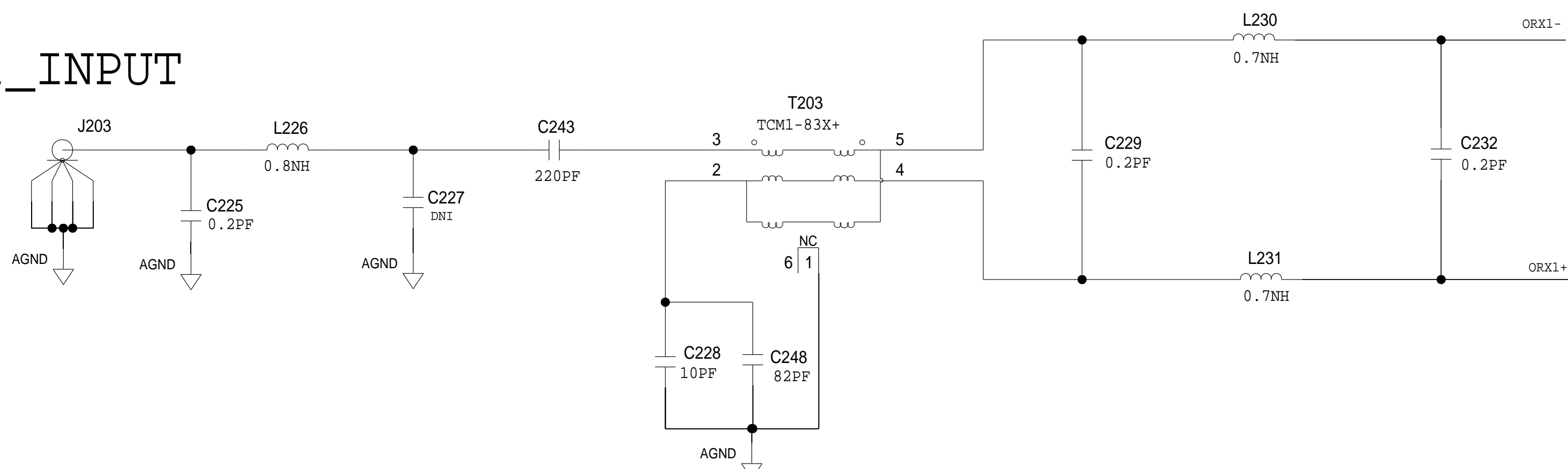
RF RX / ORX / SNIFFER INPUTS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

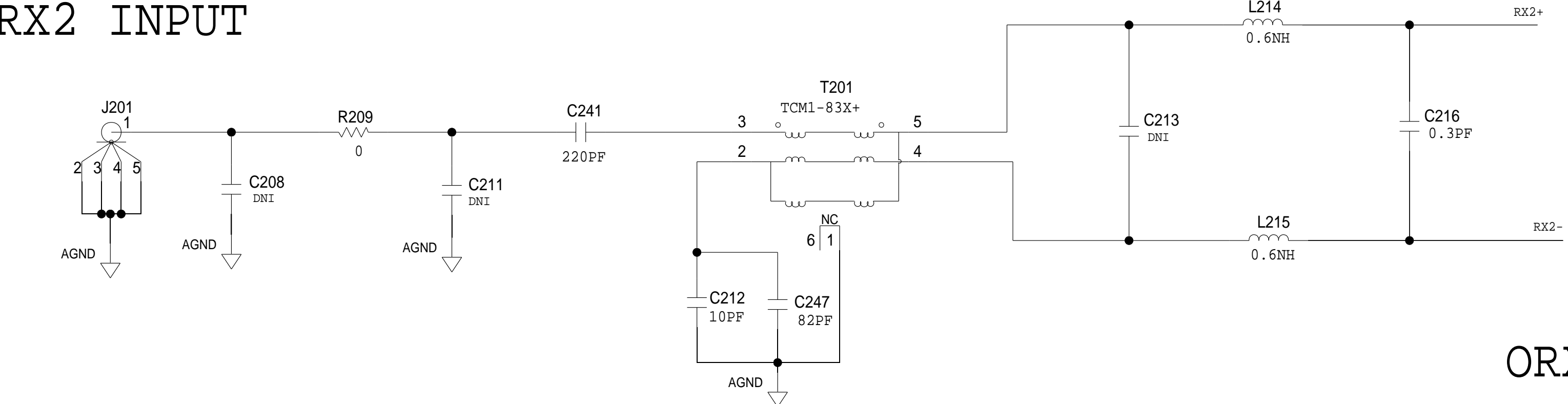
RX1 INPUT



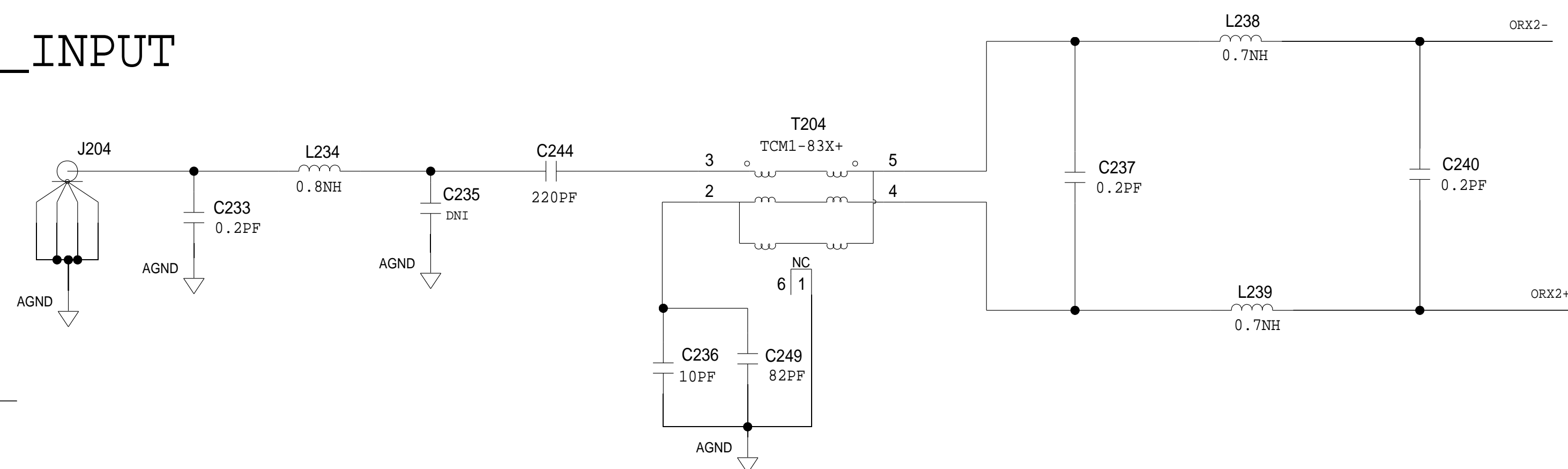
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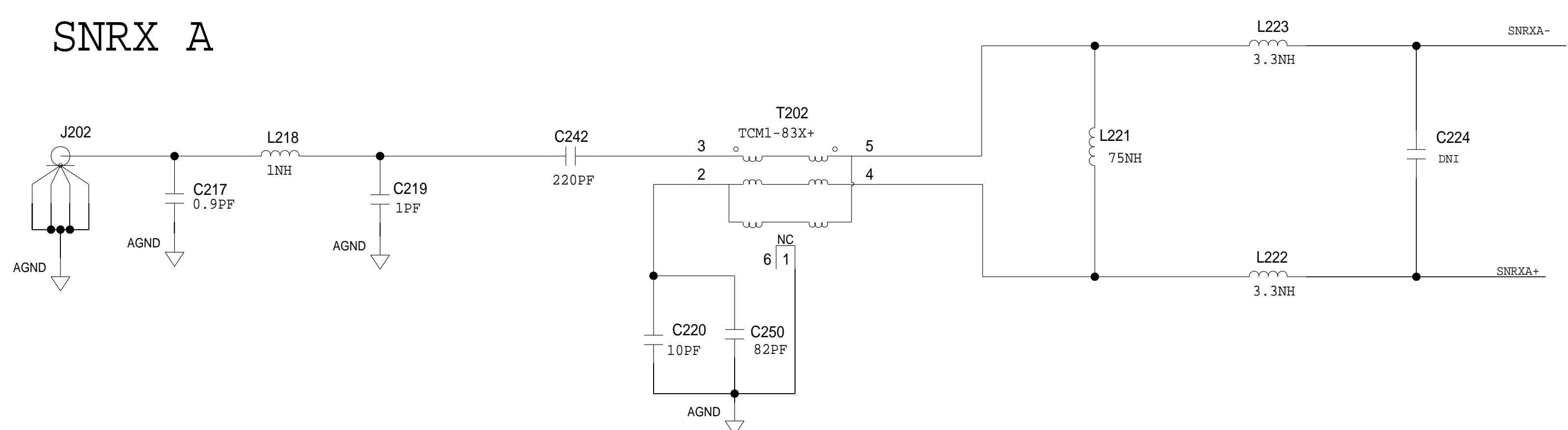
RX2 INPUT

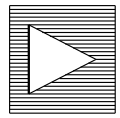


ORX2_INPUT



SNRX A

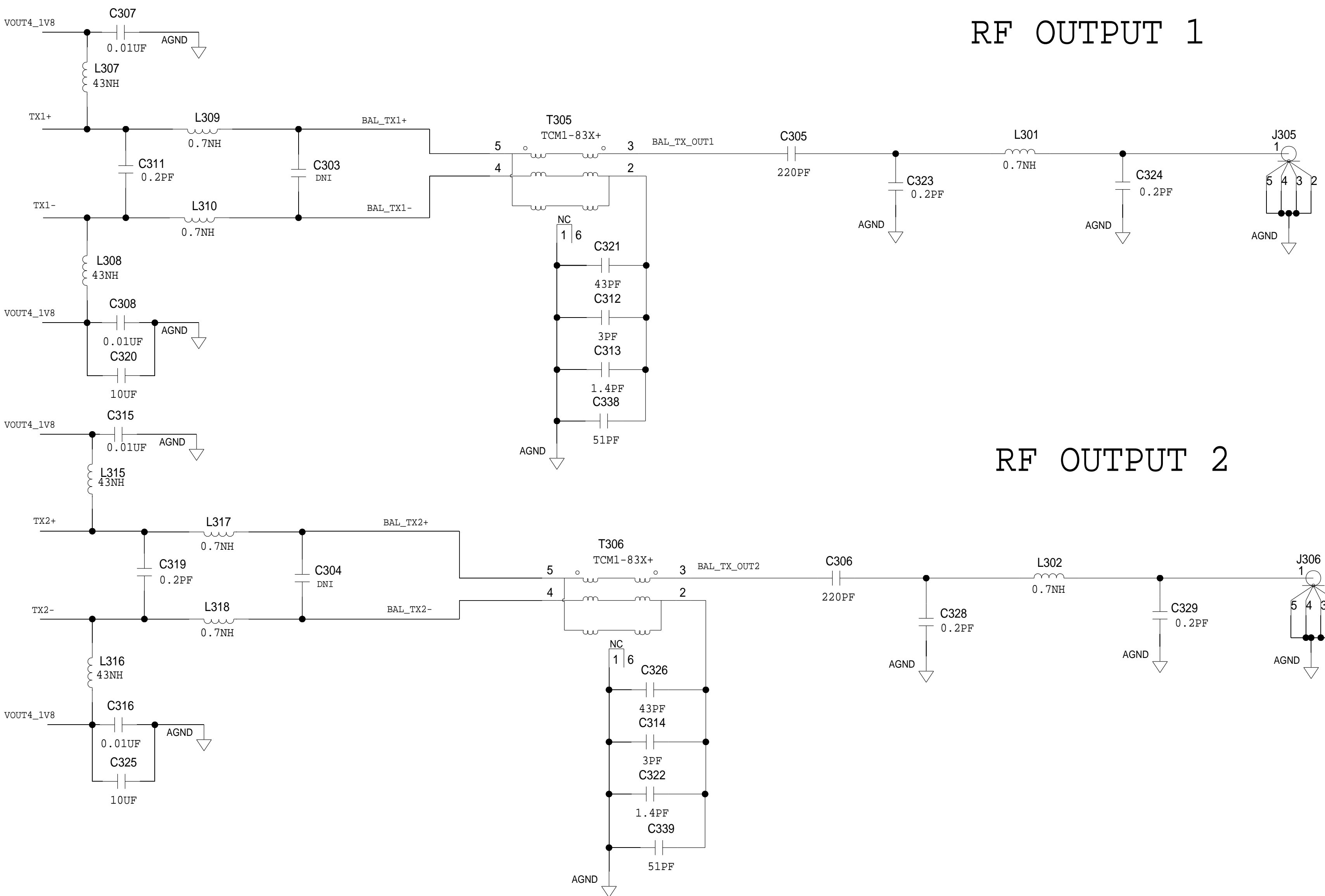
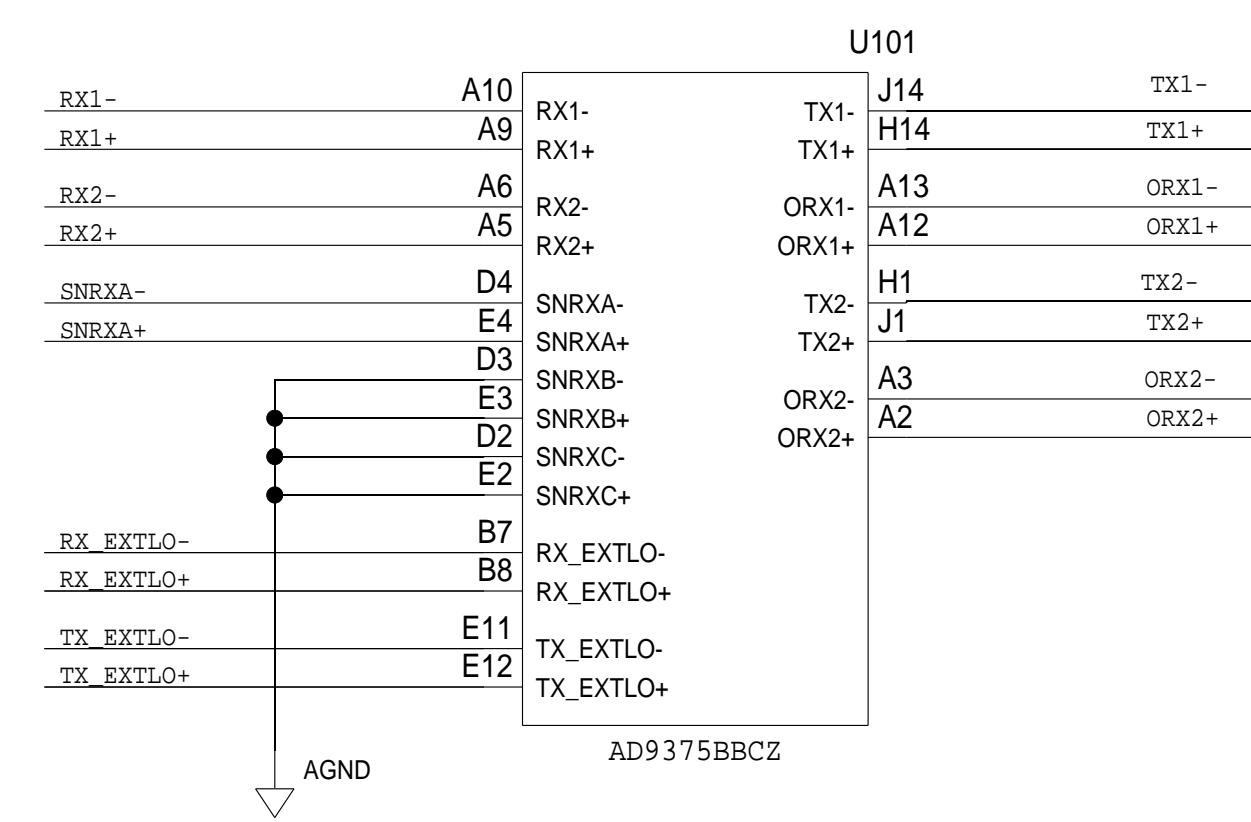


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	HW TYPE : Customer Evaluation Z Product(s): AD9375		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_047000	REV B
	PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1

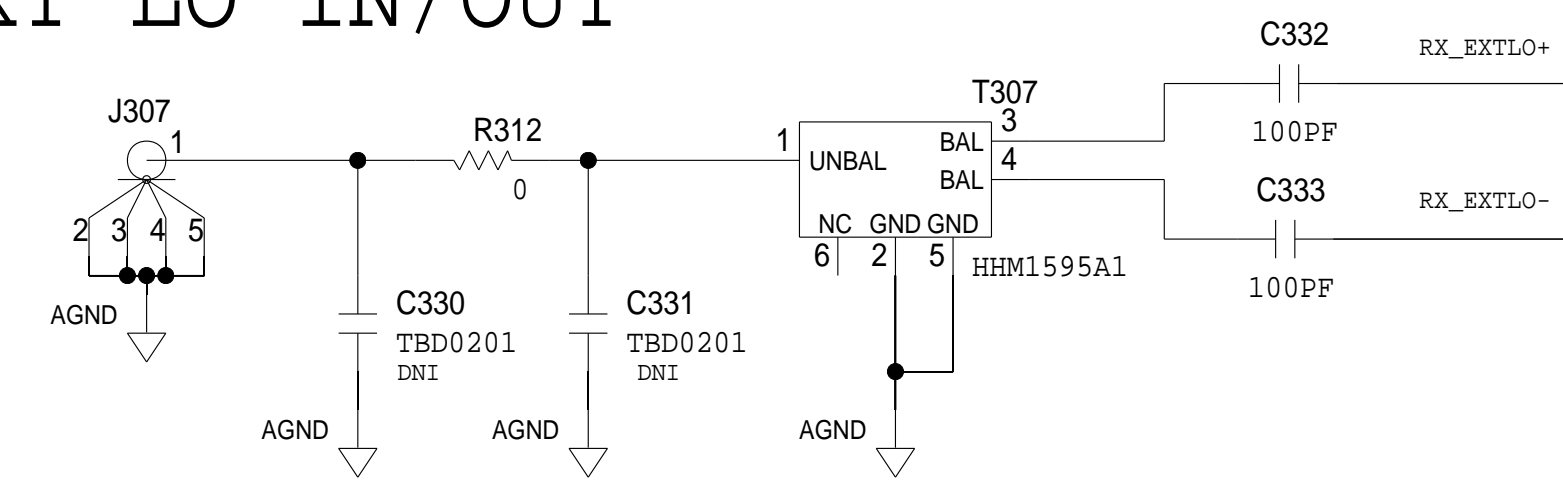
SHEET 2 OF 8

RF TX OUT / EXT LO IN

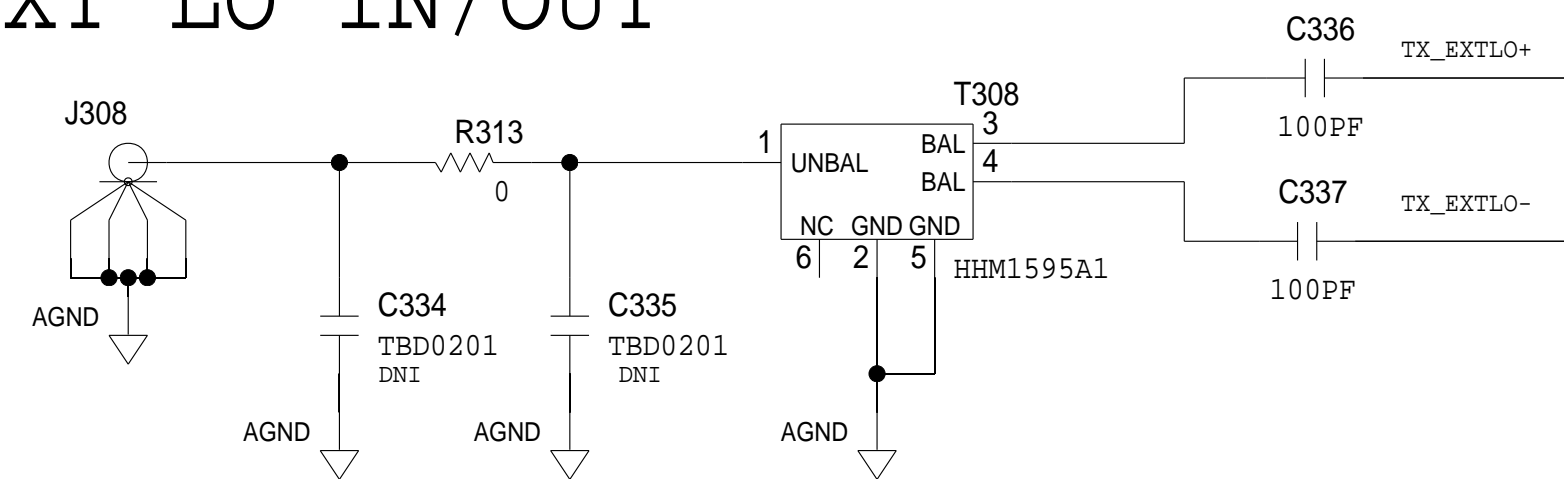
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



RX EXT LO IN/OUT



TX EXT LO IN/OUT



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		DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_047000		REV B
		PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1	SHEET 3 OF 8

CLOCK GENERATION

REVISONS

REV	DESCRIPTION	DATE	APPROVED

REF CLK

PLL1 LOOP FILTER

PLL2 LOOP FILTER

AD9528BCPZ

ADG3301BKSZ

ADG3304BRUZ

SCHEMATIC

HW TYPE : Customer Evaluation Z
Product(s): AD9375

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
T KARPUS

DRAWING NO.
02_047000

SIZE
D

SCALE
1:1

SHEET 4 OF 8

REV
B

FPGA REF_CLK+

ROUTE DIFFERENTIAL 100 OHM TRACE

FPGA_REF_CLK-

FPGA_AUX_CLK+

FPGA_AUX_CLK-

FPGA_SYSREF+

FPGA_SYSREF-

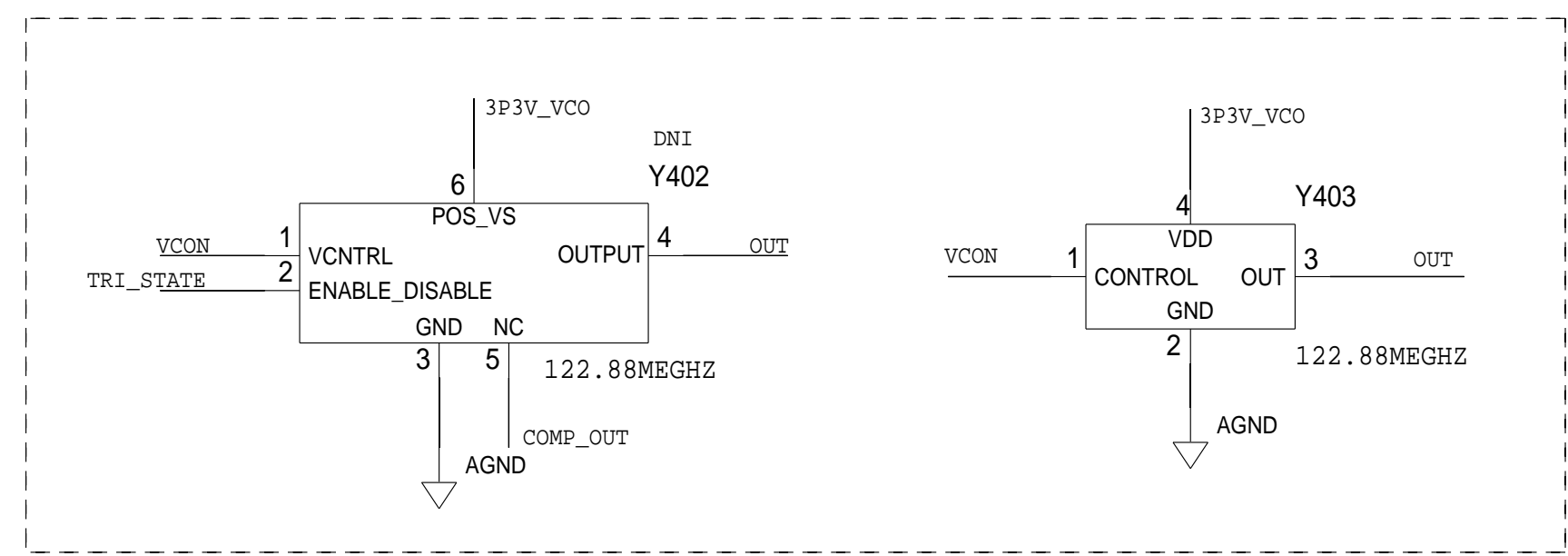
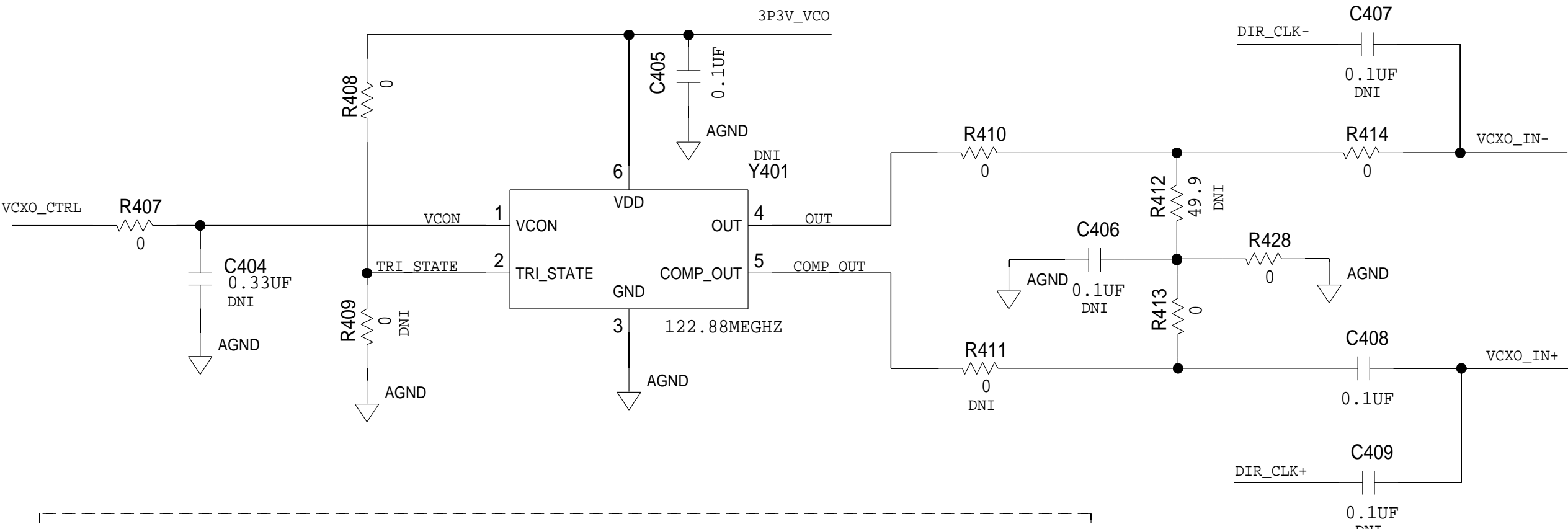
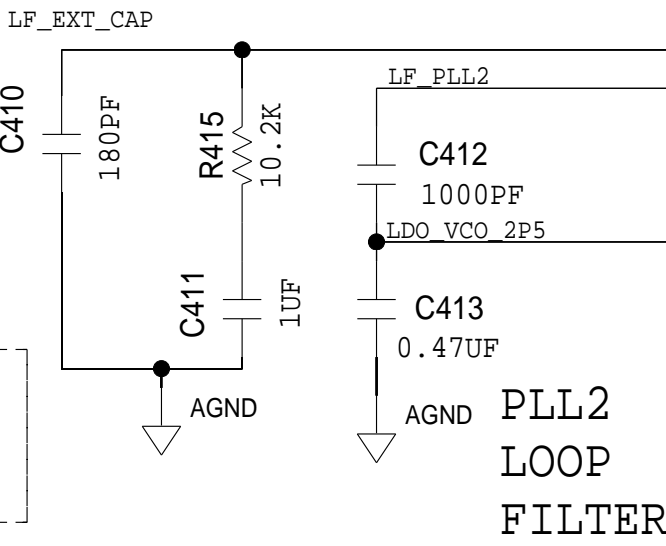
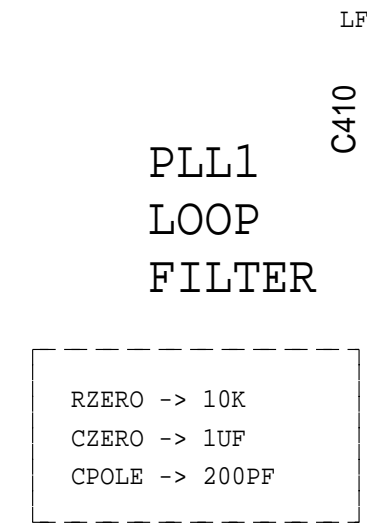
SYSREF_IN+

SYSREF_IN-

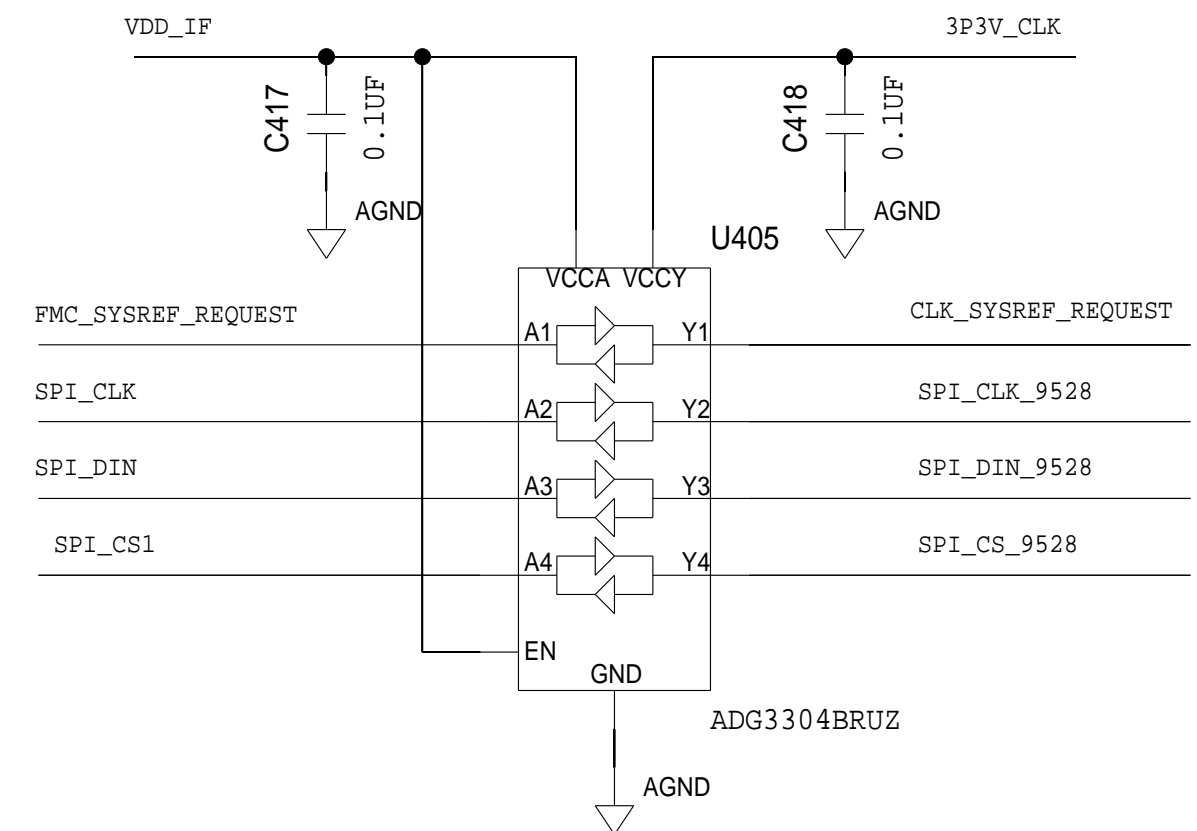
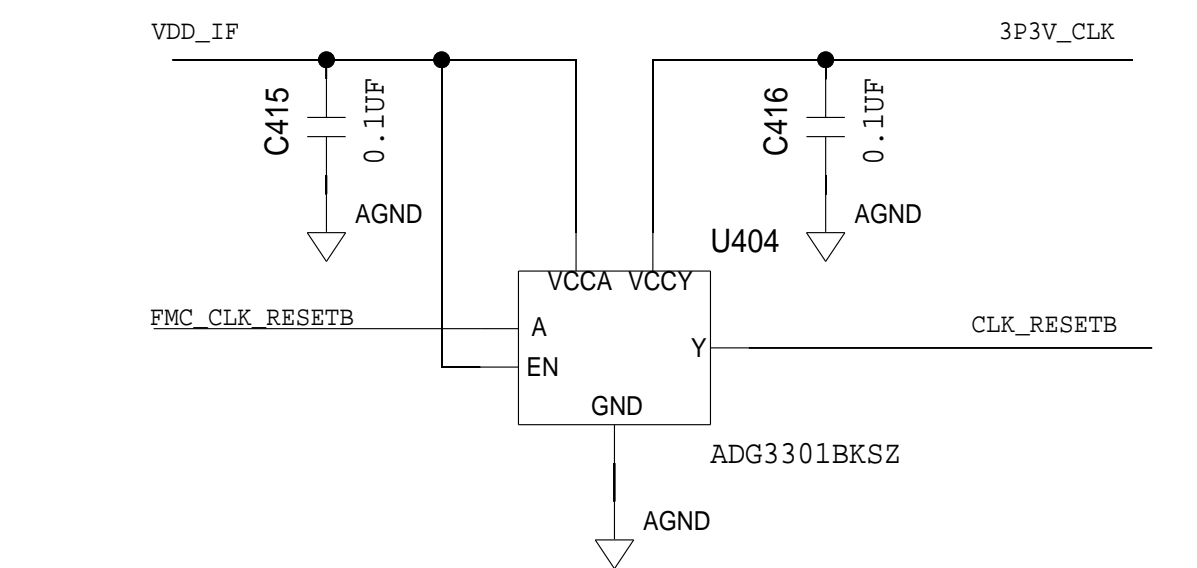
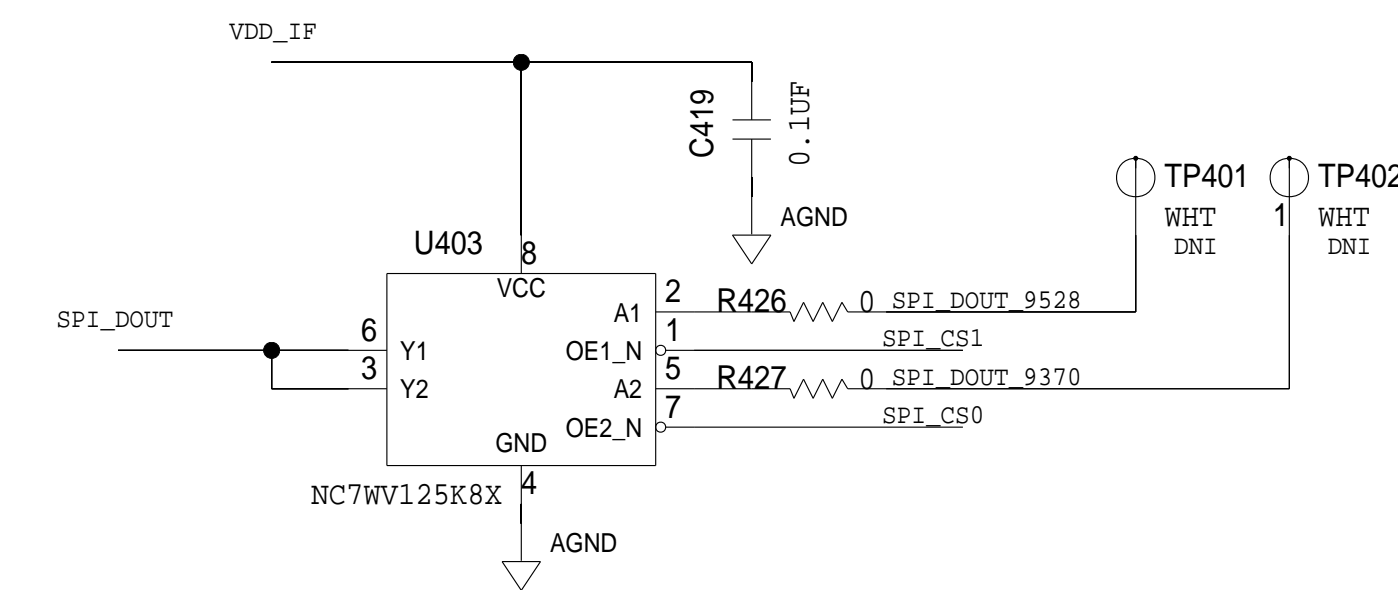
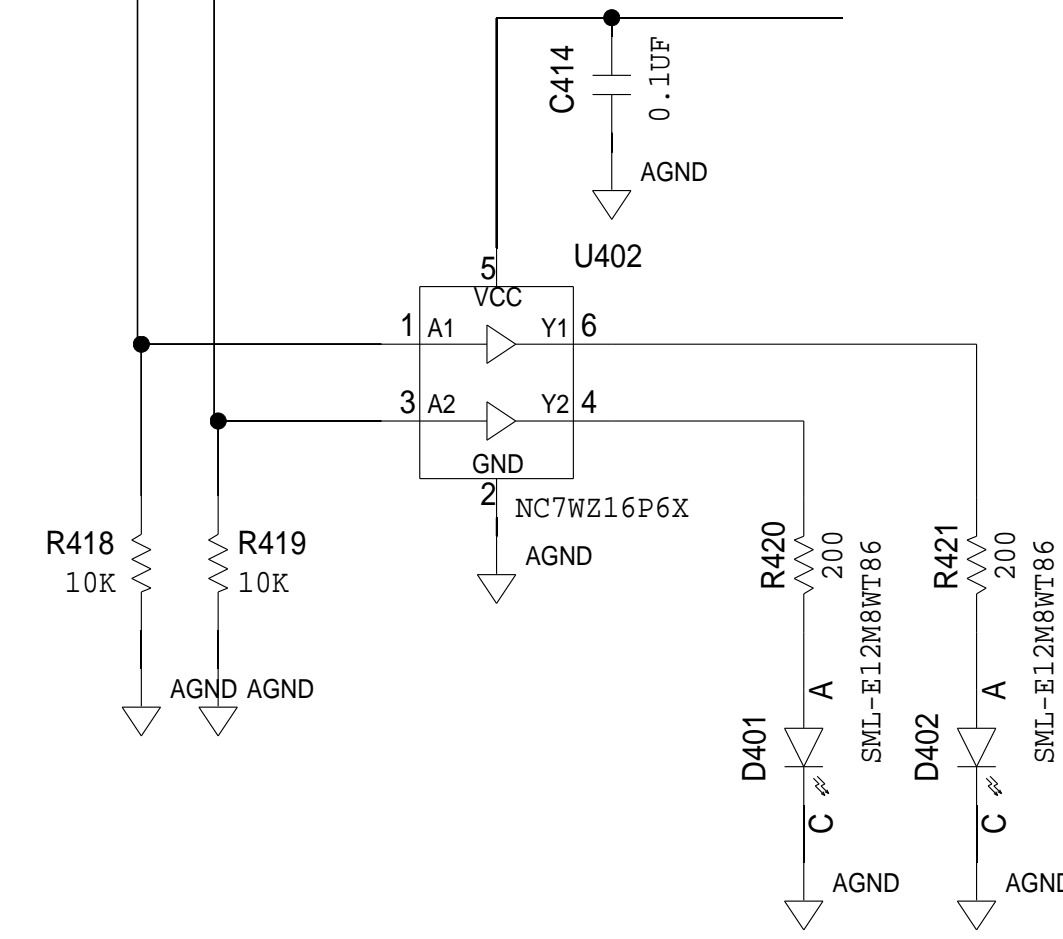
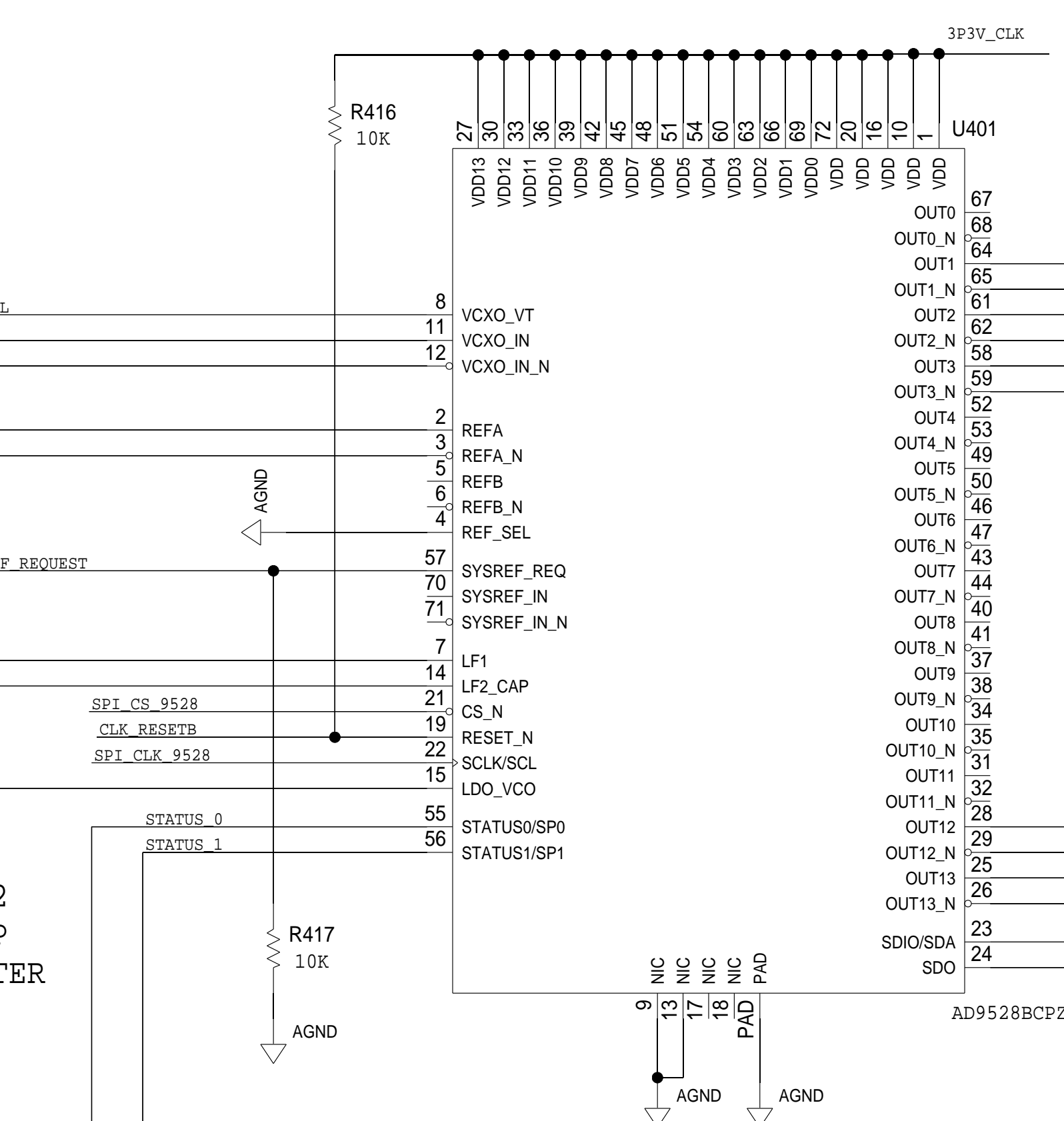
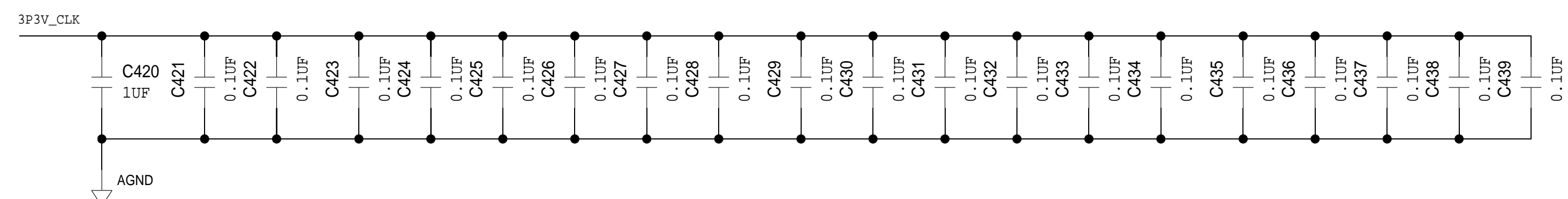
DEV_CLK_IN+


ROUTE DIFFERENTIAL 100 OHM TRACE

DEV_CLK_IN-



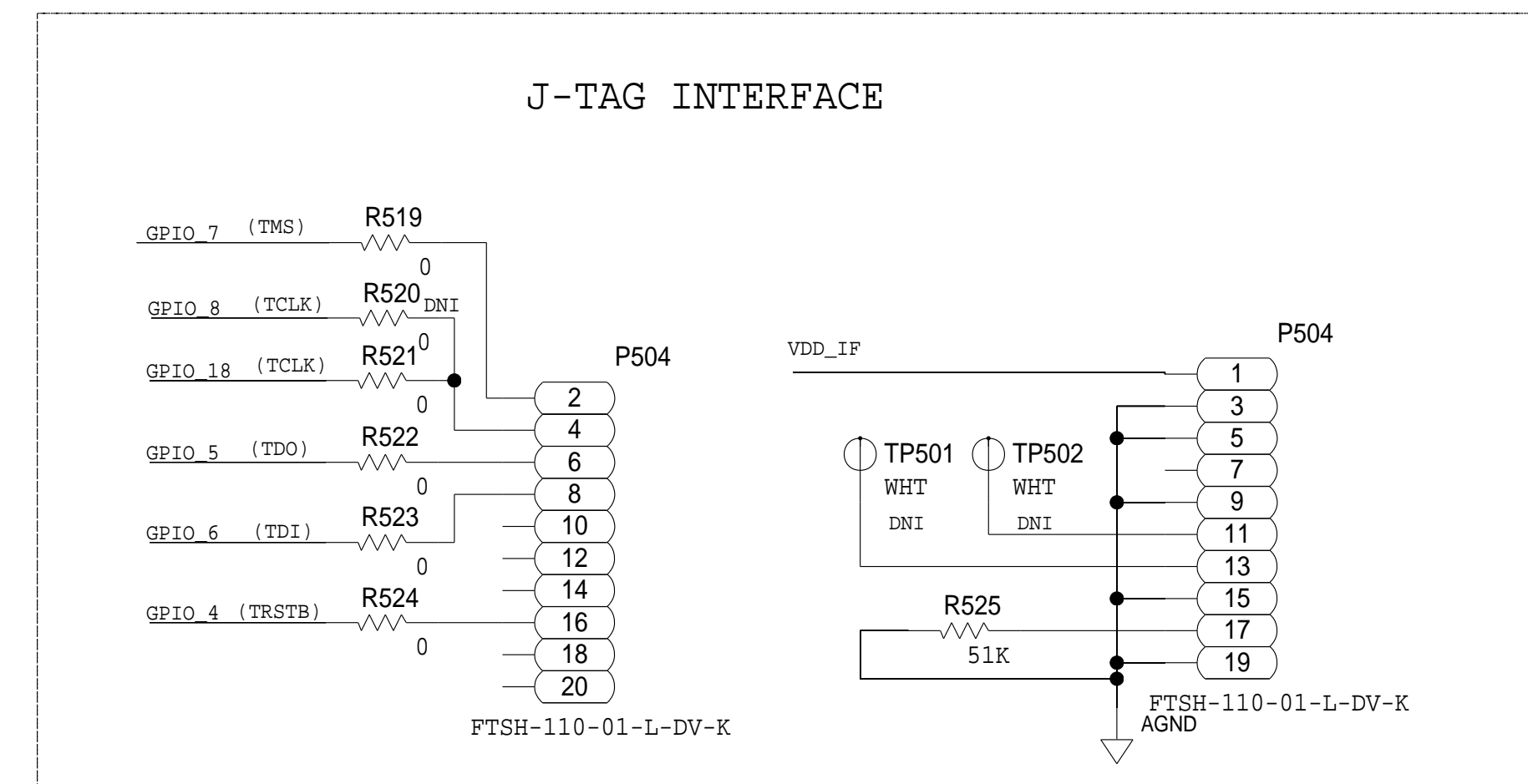
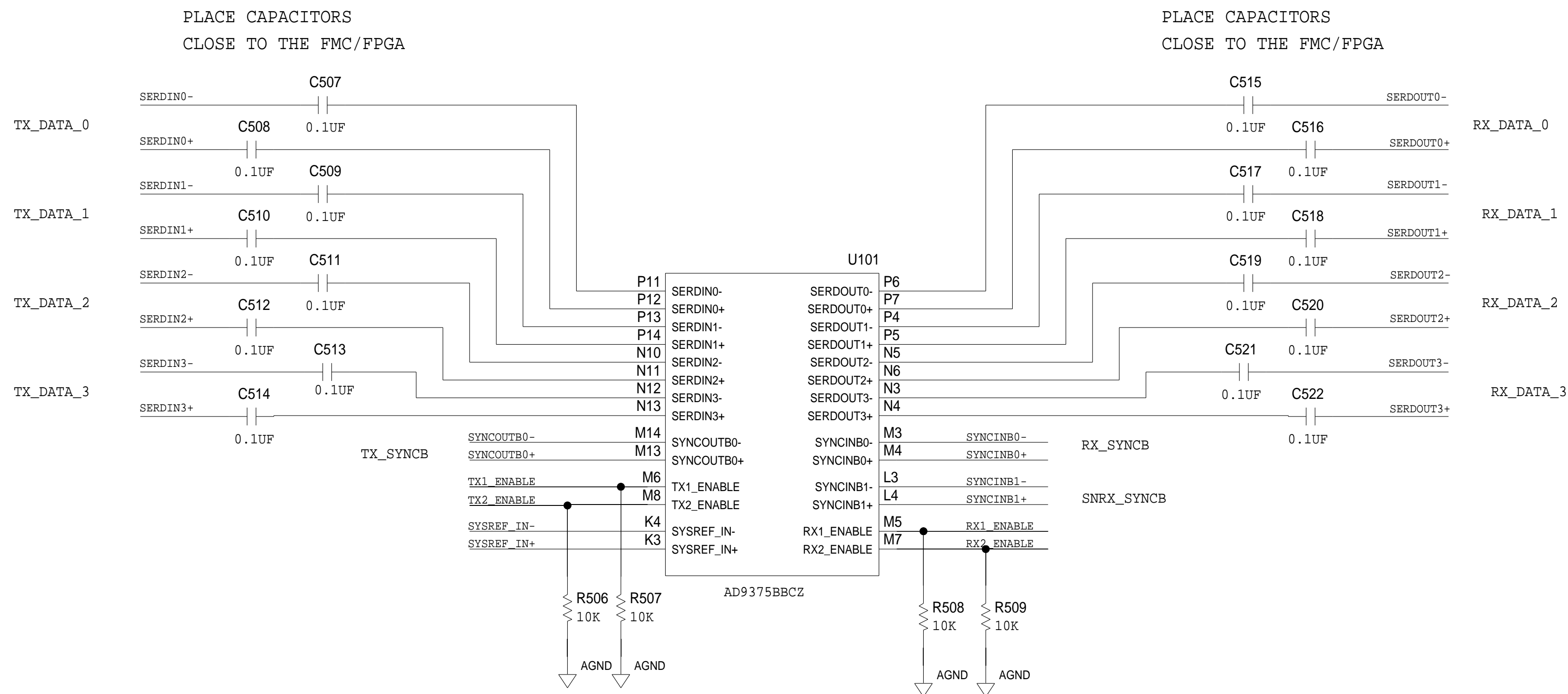
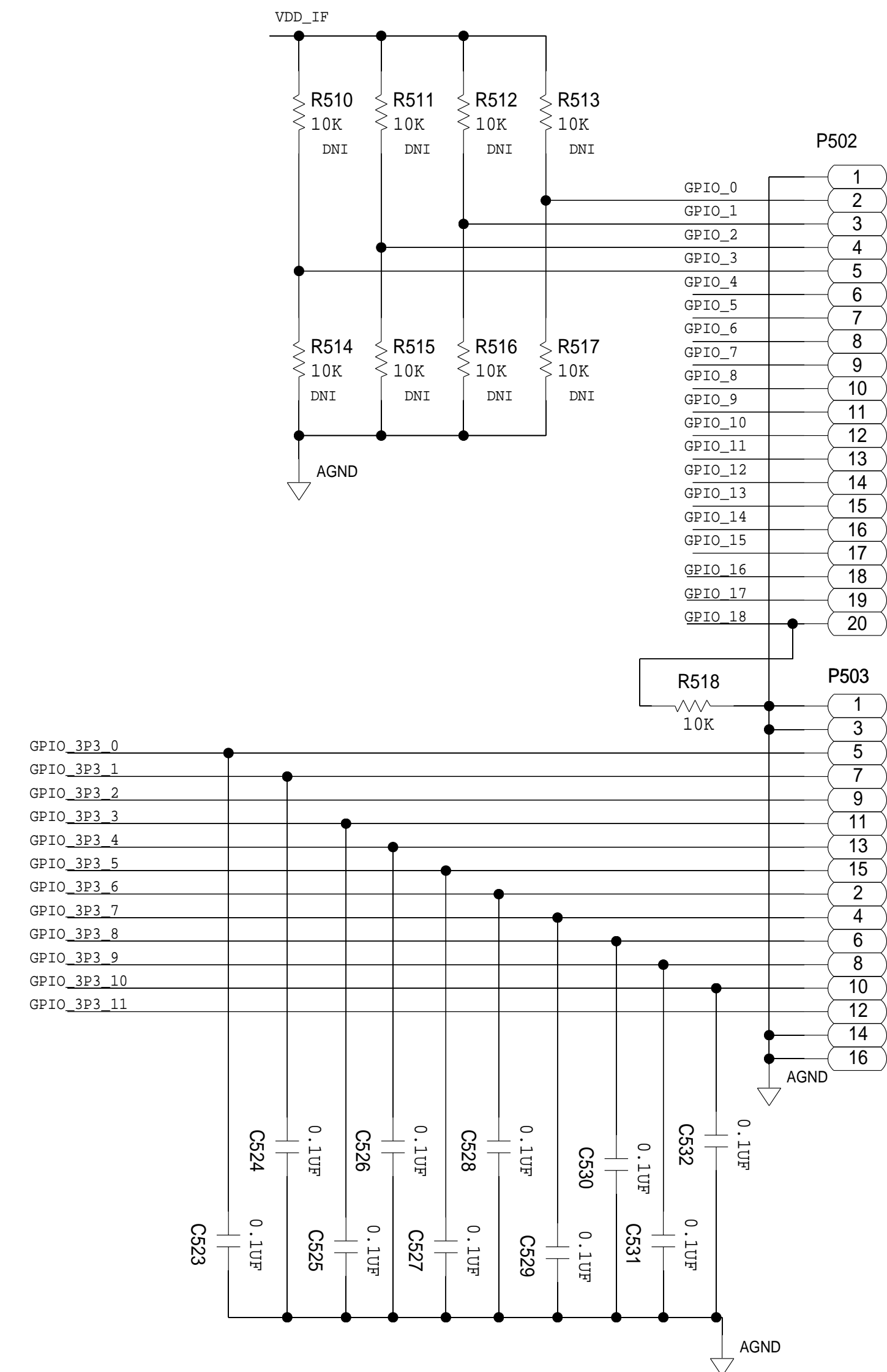
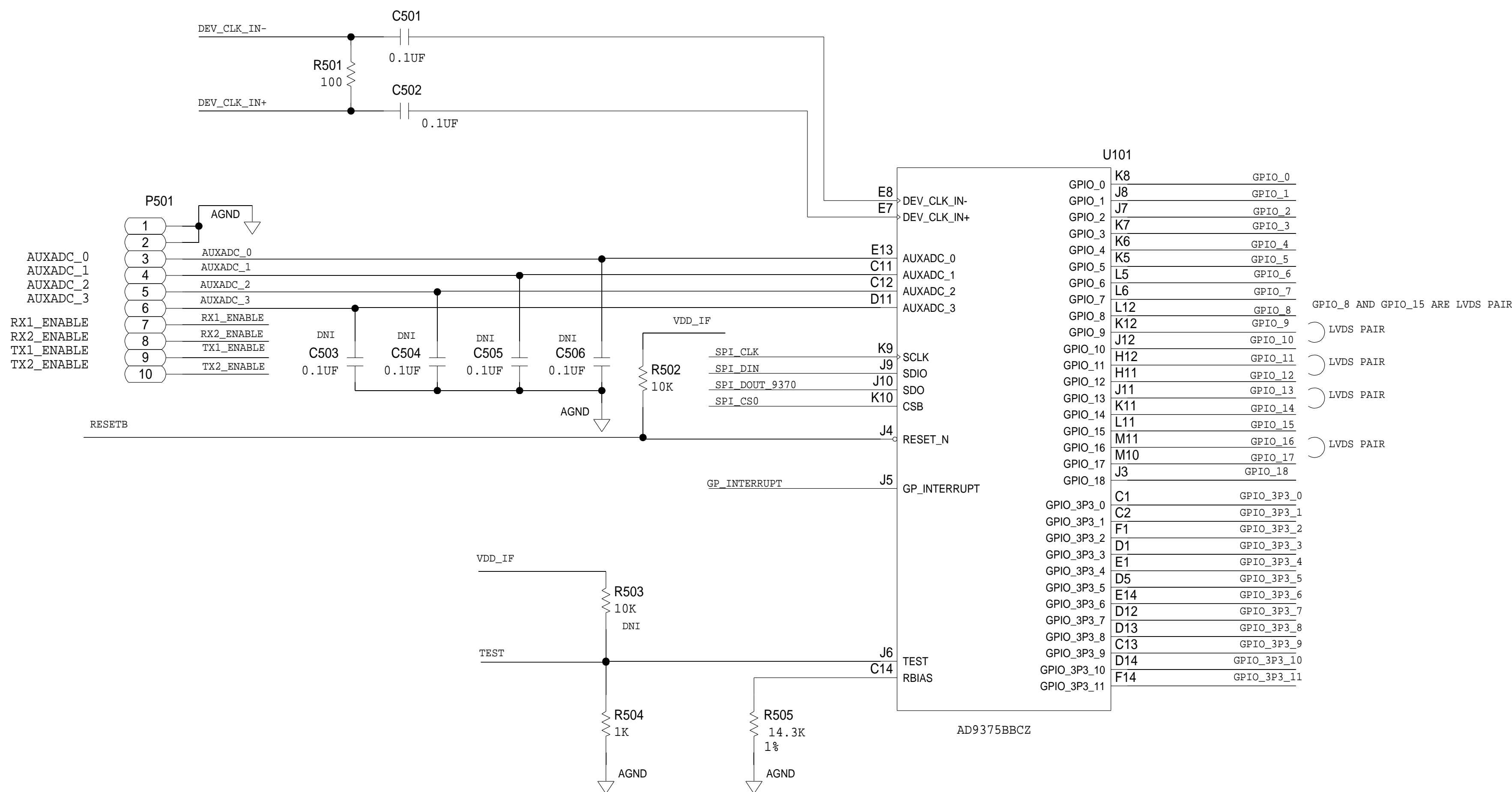
FOOTPRINTS OVERLAP IN LAYOUT
FOR CRYSTAL PACKAGE OPTION



 ANALOG DEVICES	<h1 style="text-align: center;">SCHEMATIC</h1>			
	<p>HW TYPE : Customer Evaluation Z Product(s) : AD9375</p>			
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	SIZE D	SCALE 1:1	SHEET 4	OF 8

JESD INTERFACE / GPIO / JTAG

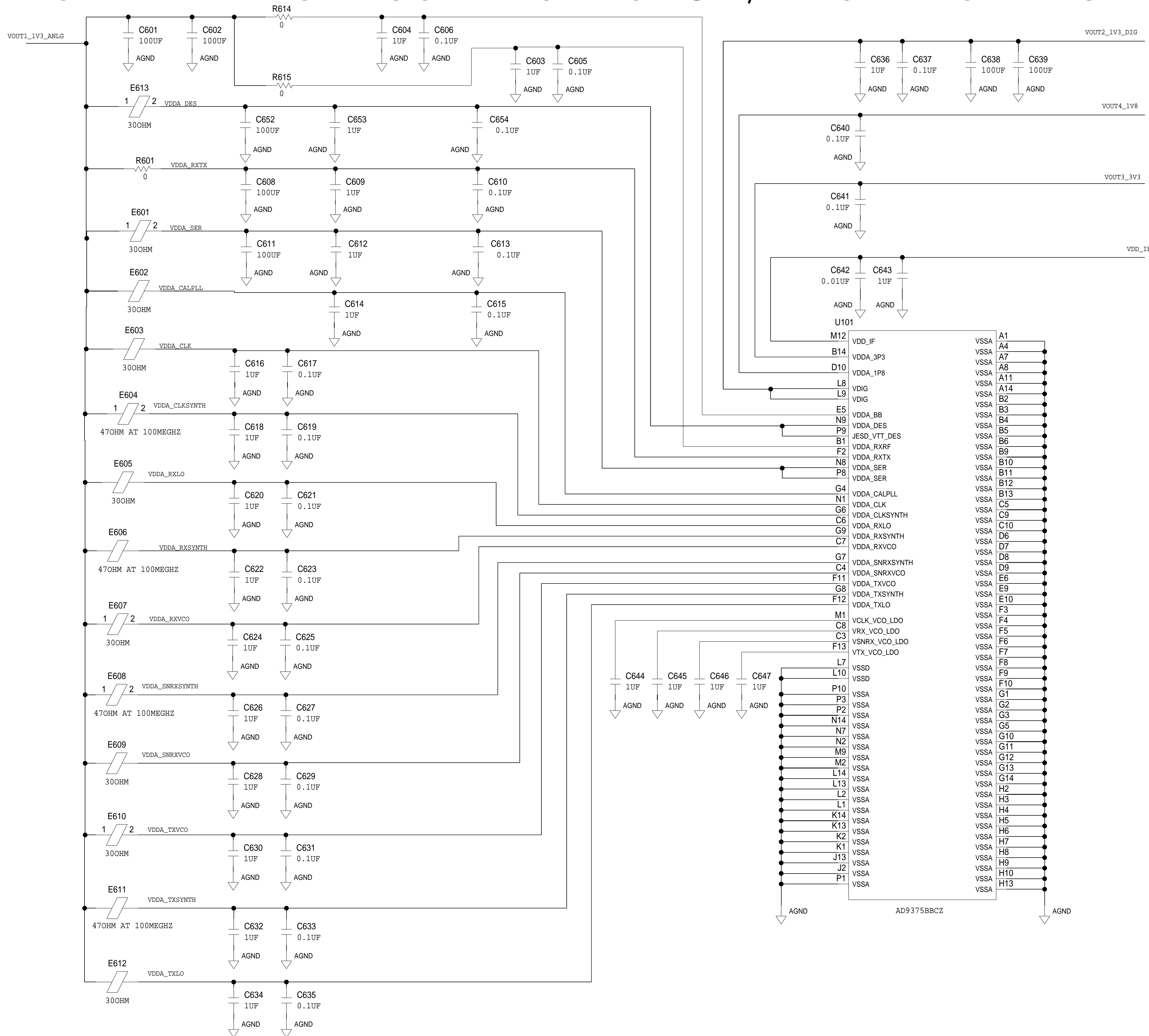
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



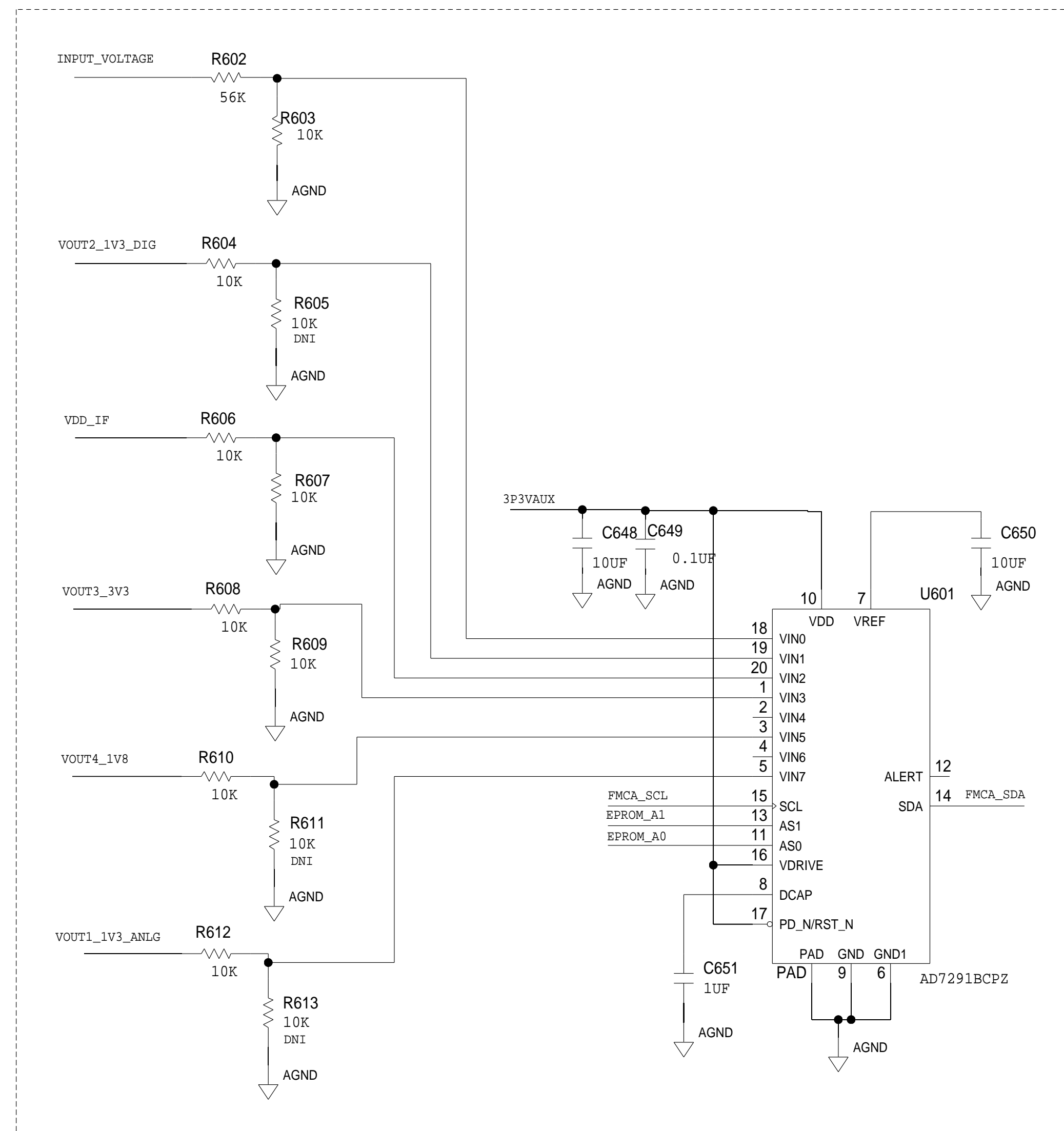
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DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02_047000		REV B	
PTD ENGINEER T KARPUS		SIZE D	SCALE 1:1	SHEET 5	OF 8

POWER - DUT CONNECTIONS / MONITORING

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



POWER DOMAINS MONITORING ADC



SCHEMATIC			
HW TYPE : Customer Evaluation Z Product(s): AD9375			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_047000	REV B	
PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1	SHEET 6 OF 8

POWER SUPPLY

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

D

C

B

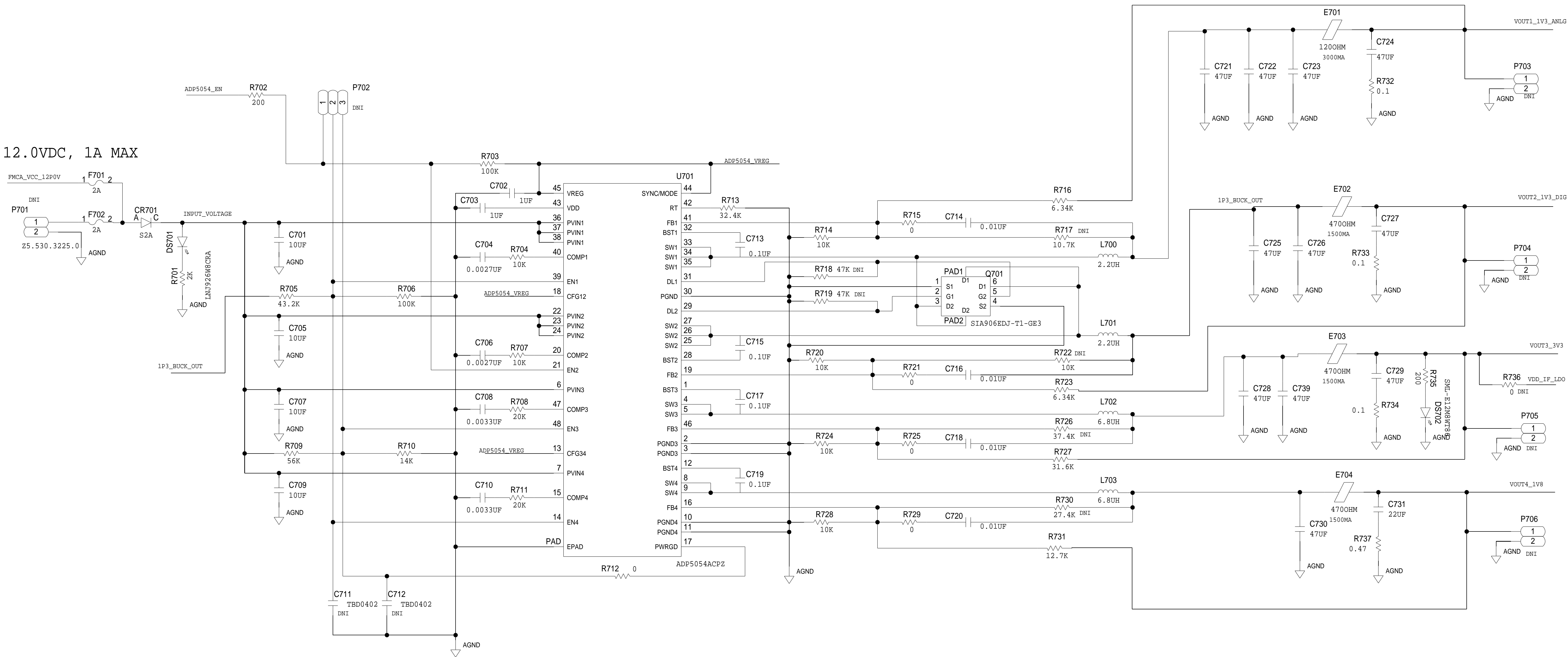
A

D

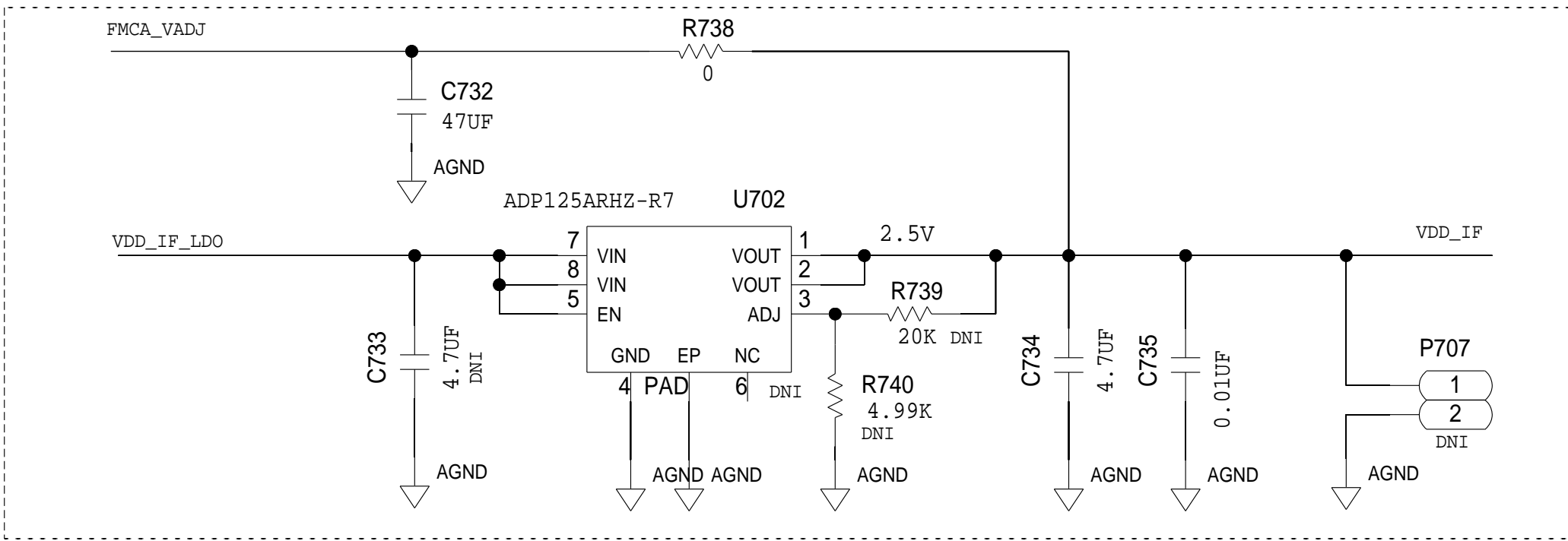
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B

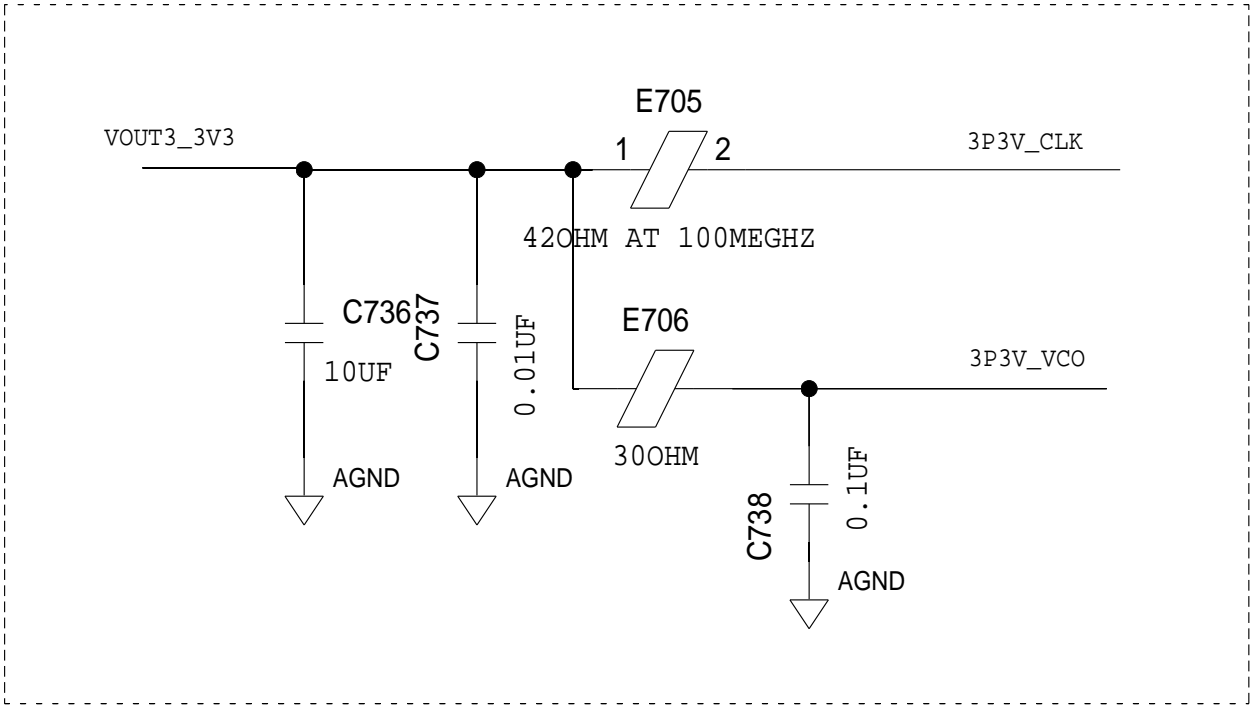
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INTERFACE SUPPLY



CLOCK SUPPLY



SCHEMATIC			
HW TYPE : Customer Evaluation Z Product(s): AD9375			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_047000	REV B	
PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1	SHEET 7 OF 8

FMC – FPGA CONNECTIONS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

D

C

D

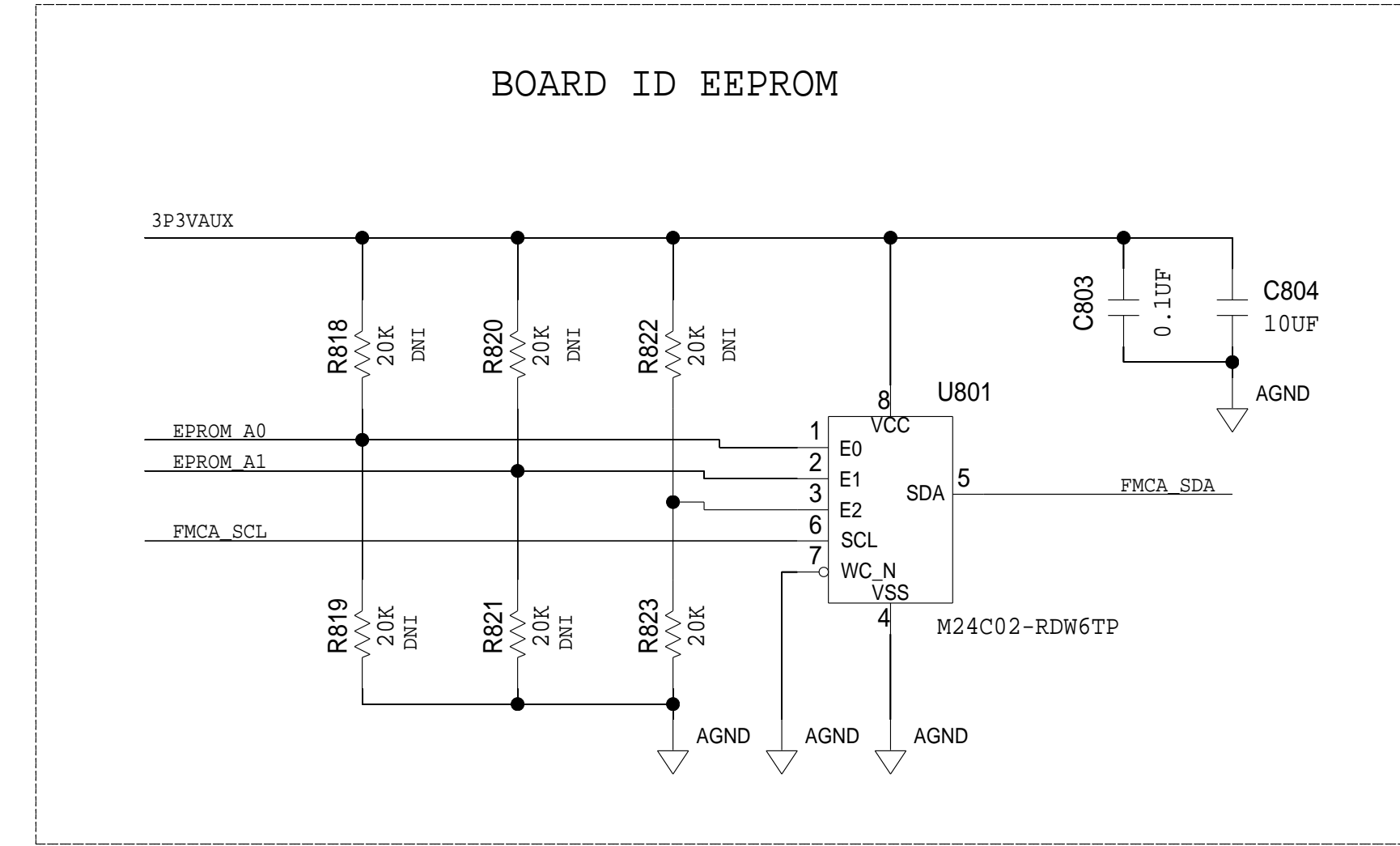
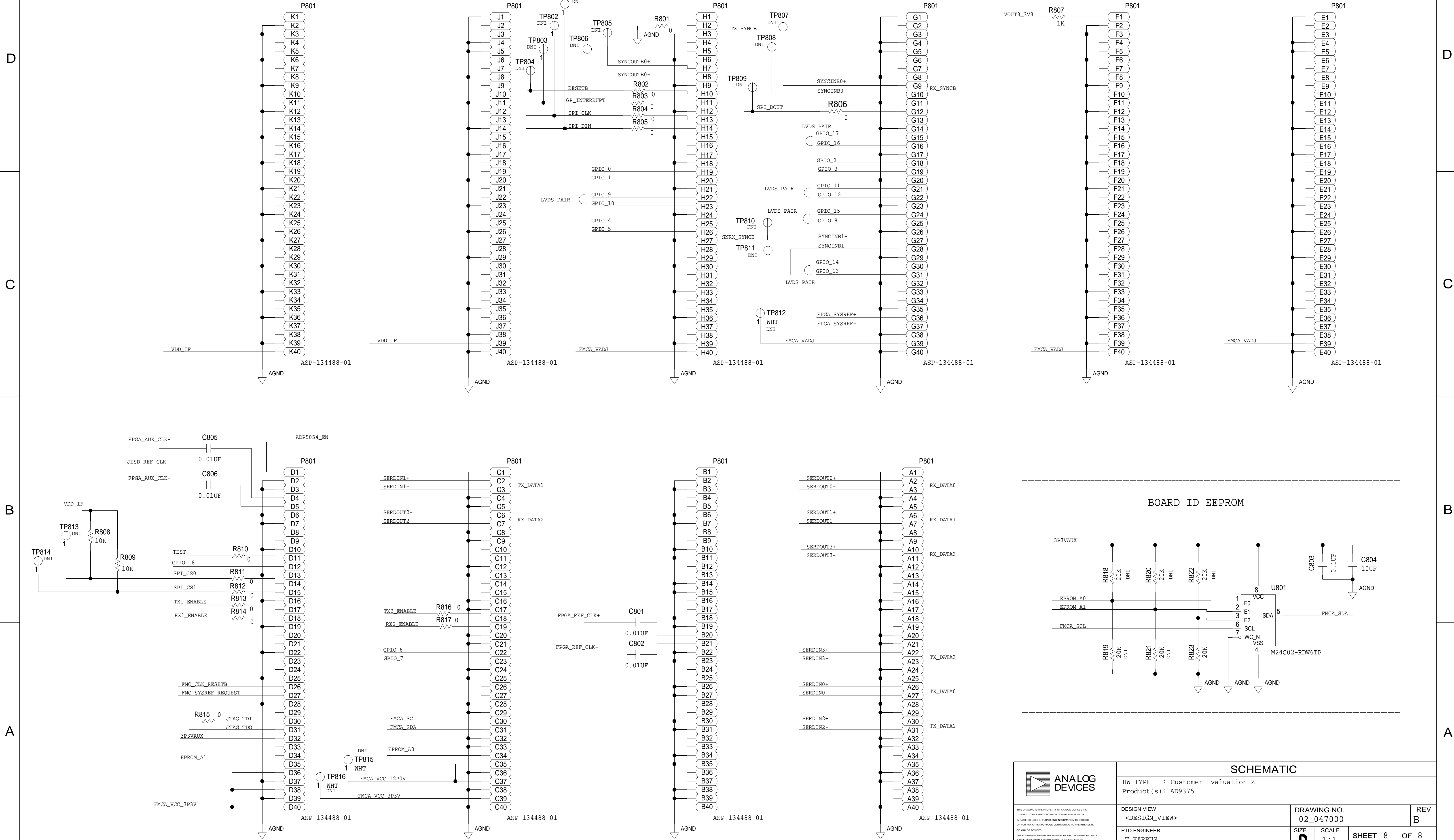
C

B

B

A

A



SCHEMATIC			
HW TYPE : Customer Evaluation Z Product(s): AD9375			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_047000	REV B	
PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1	SHEET 8 OF 8